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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,388	01/15/2004	Takeshi Kobayashi	61282-055	4950

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EXAMINER	
NGUYEN, DILINH P	
ART UNIT	PAPER NUMBER
2814	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,388	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,19,20 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,19,20 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5, 19-20 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda et al. (U.S. Pat. 6072239) (previously applied) in view of Ooyama et al. (U.S. Pat. 6191494) (newly cited for amended claims 1 and 19).

- Regarding claim 1, Yoneda et al. disclose a lead frame comprising:

a lead frame body 121 comprising a sheet-shaped body made of metal [Cu] (fig. 76, column 20, lines 42-44);

a groove portion 158 (fig. 76) for forming a lead which is formed by a predetermined depth in a lead forming region on a surface of the lead frame body; and

a lead 155 and 171 (fig. 79), wherein the lead 171 having a portion which protrudes from the groove portion laterally onto the surface of the lead frame body 121, the lead completely filling the groove portion and being made of material different (column 16, lines 19-22) from material of the lead frame body 121 (fig. 79).

Yoneda et al. do not disclose the lead having a portion so as to be in contact with the surface of lead frame body.

However, Ooyama et al. disclose a lead frame comprising: a lead 26b (fig. 5G),

or lead 28b (fig. 6) having a portion which protrudes from the groove portion laterally onto the surface of the lead frame body 31 (fig. 5A) so as to be in contact with the surface of the lead frame body (fig. 5G). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a portion of the lead so as to be in contact with the surface of lead frame body as taught by Ooyama et al. into the device structure of Yoneda et al. in order to assure in quality and reduce complexity of implementation of a chip package.

- Regarding claim 2, Ooyama et al. disclose a lead frame comprising:

  a first conductor layer 28a-2 formed in the groove portion; a second conductor layer 28b-1 formed on the first conductor layer; and a third conductor layer 28b-2 formed on the second conductor layer; wherein the first conductor layer is assembled to an assembling member, and the third conductor layer 28b-2 is assembled to a bonding pad of a semiconductor chip (fig. 6).

- Regarding claim 3, Yoneda et al. disclose that wherein the first conductor layer 155 covers an entire inner wall of the groove portion (fig. 76).
- Regarding claim 3, Ooyama et al. disclose that wherein the first conductor layer 28a-2 covers an entire inner wall of the groove portion (fig. 6).
- Regarding claim 5, Ooyama et al. disclose that the lead includes a barrier layer [Au layer 28a-1] for suppressing a reaction between the lead frame body and the first conductor layer, the barrier layer being provided between the first conductor layer and the groove portion (figs. 5G and 6).
- Regarding claim 19, Yoneda et al. disclose a semiconductor device comprising:

a semiconductor chip 111;

a multi-layer lead 113 connected to the semiconductor chip and having a first conductor layer 113C;

a piece of sealing resin 112; wherein a portion of the reverse face of the multi-layer lead protrudes from a principal plane of the piece of sealing resin 112, the first conductor layer 113C covering an entire surface of the portion and including a part within an enclosed groove of the piece of sealing resin 112 (fig. 50).

Yoneda et al. do not disclose that the multi-layer lead contacts a surface of the semiconductor chip.

However, Ooyama et al. disclose a semiconductor device comprising: a multi-layer lead 28a and 28b contacts a surface of a semiconductor chip (fig. 6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the multi-layer lead contacts a surface of the semiconductor chip as taught by Ooyama et al. into the device structure of Yoneda et al. in order to increase the contact area between the chip and the lead.

- Regarding claim 20, Yoneda et al. disclose that the multi-layer lead 113 further including: a second conductor layer laminated inside the first conductor layer 113C; and a third conductor layer formed inside the second conductor layer (fig. 50).
- Regarding claim 32, Yoneda et al. disclose that a surface of the first conductor layer 113C facing away from the semiconductor chip 111 is uncovered (fig. 59).

Response to Arguments

Applicant has amended claims 1 and 19, see the rejection regarding the currently amended claims 1 and 19 above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 5:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hoai v Pham/
Primary Examiner, Art Unit 2814

DLN